METHOD AND APPARATUS FOR SYNCHRONIZED BUSES

ABSTRACT OF THE INVENTION

A bus arbiter controls the bus frequency in a system that includes a plurality of bus masters and a plurality of slaves. The bus frequency is determined according to the internal frequency of the devices that are part of the transaction. Additionally, the bus frequency is set according to the length of the bus between the devices that are a part of the transaction and, correspondingly, the expected amount of impedance there between. As a part of the present invention, a master seeking bus resources to initiate a transaction generates a bus request and a destination address to the bus arbiter so that it may determine a corresponding bus frequency in advance. Thereafter, the bus arbiter sets the bus frequency to a value that corresponds to the transaction that is about to take place thereon. Next, the bus arbiter issues a grant signal to enable the master to use the bus. Each slave device for a transaction then generates or receives sample cycle signals indicating when a signal should be read on the bus.